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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,162	01/11/2002	Shahram Mostafazadeh	NSC1P225R	3102
22434	7590	06/29/2006	EXAMINER	
BEYER WEAVER & THOMAS, LLP			PHAM, THANH V	
P.O. BOX 70250			ART UNIT	PAPER NUMBER
OAKLAND, CA 94612-0250			2823	

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/044,162	MOSTAFAZADEH ET AL.	
	Examiner	Art Unit	
	Thanh V. Pham	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 June 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 4-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 4-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|-----------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Response to Amendment

Duplicate Claims

1. Applicant is advised that should claim 9 be found allowable, newly added claim 14 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof.

When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k). In this instance, throughout the arguments of record, the limitation of "the exposed lower surfaces of the leads" in claim 14 is not different from the limitation of "the exposed portion of the leads" in claim 9.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1 and 4-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. US 5,200,362 in combination with Ogawa et al. US 5,252,855.

Re claim 1, the Lin et al. reference discloses a method for producing an electrical device (figs. 1-5 and 9) comprising the steps of:

forming a flat lead frame 13 including a plurality of leads extending radially from a central (fig. 9), the lead frame having opposing upper and lower surfaces (col. 2, lines 51-54);

mounting the lead frame 13 and an integrated circuit die 15 onto a strip of adhesive tape 12 such that the die is located in the central, and the lower surface of the lead frame contacts the adhesive tape (fig. 2);

electrically connecting bond pads on a top surface of the die to associated lead frame leads using wire bonding 18;

forming a plastic casing 20 over an upper surface of the die and the upper surface of the lead frame wherein the plastic casing (comprising molding plastic onto the upper surfaces of the die and the lead frame, *re claim 6*) comes into contact with the adhesive tape such that a lower surface of the plastic casing is substantially co-planar with the lower surfaces of the lead frame (fig. 3, col. 3, lines 13-32); and

removing the adhesive tape 12 after forming the plastic casing to expose the lead frame, whereby exposed surfaces of the lead frame directly form the only externally exposed and accessible I/O contacts for the package and plastic material fills at least portions of gaps between adjacent leads, such that the lower surface of the package is substantially co-planar and includes exposed portions of the plastic casing and the lead frame (fig. 4, col. 3, lines 33-38 and col. 4, lines 55-62).

The Lin et al. method does not use a lead frame with a central opening.

The Ogawa et al. reference discloses a method of packaging an integrated circuit, fig. 5, comprising:

providing a lead frame including a plurality of leads 1 *and a central opening*, the lead frame is made by punching (*re claim 5*) or by etching (*re claim 4*) a plate composed

of a copper alloy or an iron alloy (col. 1, lines 13-16) having opposing upper and lower surfaces;

mounting the lead frame 1 and an integrated circuit die 4 onto a strip of adhesive tape 2 as element mounting member such that a lower surface of the die contacts the adhesive tape and the die is located in the central opening and the lower surface of the lead frame also contacts the adhesive tape such that the lower surface of the die and the lower surface of the lead frame are substantially co-planar;

electrically connecting bond pads on a top surface of the die to associated lead frame leads with thin metal wire 5 with the adhesive tape in place such that the adhesive tape holds the die and lead frame in place during the wire bonding operation (fig. 5 and col. 4, line 66 to col. 5, line 20).

The Ogawa et al. reference does not teach forming a plastic casing over an upper surface of the die and the upper surface of the lead frame, and removing the adhesive tape after molding the plastic casing.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the method of Lin et al. with a lead frame with a central opening of Ogawa et al. because the lead frame of Ogawa et al. would provide the formed package of Lin et al. with the die being hold during electrical connection and a thinner thickness product.

Alternatively, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the method of Ogawa et al. with a plastic casing

because the plastic casing would provide the process of Ogawa et al. with complete semiconductor package device.

The combination using a flat lead frame with central opening would produce *an encapsulated semiconductor die package* wherein the molded plastic casing comes into contact with the adhesive tape such that a lower surface of the plastic casing is substantially co-planar with the lower surfaces of the lead frame *and the die*; and removing the adhesive tape after molding the plastic casing would expose the lower surfaces of *the die* and the leads, whereby exposed portions of the leads form *the only external accessible I/O contacts for a resulting integrated circuit package* and plastic material fills at least portions of gaps formed between adjacent leads such that the lower surface of the package is substantially co-planar and includes exposed portions of the plastic casing, the lead frame and the die.

Re claim 7, the combined method discloses all claimed limitations.

Re claim 8, the formed encapsulated semiconductor die package by the combination which results in no die-support element would provide the lower surface of the die being in direct contact with a heat sink formed on the circuit board when mounted on a circuit board. (*The Lin et al. reference discloses (col. 3, lines 50-63) "exposed on one side of the resin body are portions of one side of the pattern of conductive traces 13. These conductive traces can be directly contacted for making electrical contact to the semiconductor device die", "device die 15 is mounted, can be contacted by a heat sink (not shown) in order to conduct heat away from the die during operation".*.)

Re claims 9-10 and 13-14, the Lin et al. reference further discloses (col. 4, line 30) "traces may be coupled together with solder bumps" so that it can be mounted on a circuit board.

Re claims 11-12 and 15, the Lin et al. reference further discloses (col. 4, lines 63-65) "either before or after the transfer film is removed, the traces can be severed along the lines 54 to electrically disconnect the individual devices". Based on this passage and fig. 5 the leads are trimmed and the peripheral portions of the leads are flush or substantially flush with side surfaces of the plastic casing.

Response to Arguments

4. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

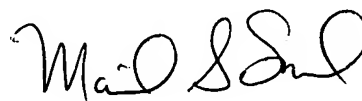
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh V. Pham whose telephone number is 703-308-2543. The examiner can normally be reached on M-T (6:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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06/22/2006



MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800